AARON T. STILLMAKER, PhD

Electrical and Computer Engineering Department
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RESEARCH INTERESTS

High speed low-power many-core processor architecture and physical design, VLSI design, digital circuit design, hardware optimization, Verilog hardware design, parallel algorithms, embedded system design, system on chip (SoC) design, and many-core network on chip (NoC) design.

EDUCATION

University of California, Davis, CA
Ph.D. in Electrical and Computer Engineering: 2015
Major: Digital Design and Computer Systems**,** Minor: Signals and Systems
Advisor: Bevan M. Baas, PhD
Dissertation: "Design of Energy-Efficient Many-Core MIMD GALS Processor Arrays in the 1000-Processor Era."

University of California, Davis, CA
M.S. in Electrical and Computer Engineering: 2013

California State University, Fresno, CA
B.S. *magna cum laude* with honors in Computer Engineering, minor in Business: 2008
Smittcamp Honors College *President's Scholar*

PROFESSIONAL EXPERIENCE

California State University, Fresno, CA *Spring 2017 - Present*

Assistant Professor
Electrical and Computer Engineering Department

I am a tenure-track professor in the Lyles College of Engineering at California State University, Fresno, teaching 3 courses (~9 WTUs) a semester. Details are given in the *Teaching Experience* section.

California State University, Fullerton, CA *Fall 2016*

Assistant Professor
Computer Engineering Program

I was a tenure-track professor in the College of Engineering and Computer Science at California State University, Fullerton, teaching 3 courses (~9 WTUs) a semester. Details are given in the *Teaching Experience* section.

University of California, Davis, CA *Winter 2016*

Lecturer
Department of Electrical and Computer Engineering

I was the instructor of record for EEC 281, VLSI Digital Signal Processing, which is a 4 unit, graduate course for the department with a course enrollment of 12 students. Details are given in the *Teaching Experience* section.

University of California, Davis, CA *Fall 2015*

Associate Instructor
Department of Electrical and Computer Engineering

I was the instructor of record for EEC 116, VLSI Design, which is a 4 unit, upper division, elective design course for the department, supervising two teaching assistants with a course enrollment of 30 students, including 9 graduate students. Details are given in the *Teaching Experience* section.

University of California, Davis, CA *2008 – 2015*

Graduate Student Researcher
VCL, Department of Electrical and Computer Engineering

While in the VLSI Computation Laboratory (VCL), I have worked on a number of research projects, culminating in being the lead physical layout designer of our group's 3rd generation and 4th generation a many-core processor array, working with Cadence, Synopsis, and Mentor Graphics CAD tools. The details of the new processor array were recently published in the VLSI Symposium and HotChips, with two invited journal papers currently under review. The 3rd generation chip, named KiloCore, contains 1,000 processor cores, the most general purpose processing cores on one fabricated die that we are aware of. Each core runs a reduced instruction set, contains its own oscillator for fine-grained frequency scaling, nearest-neighbor communication with dual clock FIFOs to cross clock boundaries, and a simple packet switched router. The 4th generation many-core array, which recently taped out, will contain architectural enhancements, dynamic voltage scaling, and application specific accelerators.

In the past, I have worked on creating low-energy, high-throughput sorting algorithms for fine-grained many-core processing arrays, coding in our own Assembly Language as well as C++ and CUDA. The preliminary results of this project were published in the IEEE International Conference on Parallel and Distributed Systems in 2013, SRC's TECHCON 2013, as well as annual reviews for C2S2 and SRC. I have also broadened my depth with projects on transistor scaling models into the deep sub-micron regime, parallel enterprise applications, and optically networked database systems. I also wrote a dual clock FIFO in Verilog for communicating between two clock frequencies. I have also done research in the use of a fine-grained many-core processor arrays for enterprise workloads.

University of California, Davis, CA *2011 – 2013*

Teaching Assistant
Department of Electrical and Computer Engineering

I served as a Teaching Assistant in five separate courses ranging from 21 to 177 students. Details are given in the *Teaching Experience* section.

Intel, Circuit Research Lab, Hillsboro, OR *September – December 2013*

Graduate Technical Intern
An internship to work on future Network on Chip research in Intel Labs with the Circuit Research Lab (CRL) in the High Performance Circuit Research group. The work will soon be submitted as an application for a US patent.

California State University, Fresno, CA *2007 – 2008*

Teaching Assistant
Department of Electrical and Computer Engineering

I served as a Teaching Assistant for a lab class for two semesters. Details are given in the *Teaching Experience* section.

Pelco, Clovis, CA *2006 – 2008*

Software Test Specialist (Internship)
Tested Software for new digital video recording devices, created back-end scripts to run tests on programs, wrote automated testing scripts, and worked with developers to fix problems.

TEACHING EXPERIENCE

Assistant Professor, California State University, Fresno

ECE 118 Microprocessor Architecture and Programming *Spring 2017*

I am the instructor of for the department's processor/microcontroller assembly language course. This course teaching an introduction to microprocessor software, hardware, and interfacing. Emphasis is placed on learning assembly language programming, microprocessor architecture, and its associated peripherals. Microcontrollers are discussed, including microcontroller programming model and instruction set, assembler directives, writing and debugging microcontroller assembly language routines, microcontroller memory system, microcontroller communication systems. Microcontrollers are widely used in modern society with applications ranging in sophistication from simple toys to implantable medical devices. In this course, students will learn the principles of microcontrollers and learn how to use microcontrollers to implement digital systems. The primary microcontroller used in this course is the PIC16f1937.

ECE 118L Microcontroller Laboratory *Spring 2017*

I am the instructor of for the department's microcontroller laboratory course. This Lab is intended to solidify and build upon the ECE 118 course. Experiments are performed on a microcontroller and its associated peripheral I/O subsystems. Hands-on program controlled I/O, timer, parallel and serial I/O communications, A/D and subsystem interfacing is accomplished in a hands-on manner. The laboratory culminates in a final design project using the microcontroller. The primary microcontroller used in this course is the PIC16f1937, which is on a PIC Development Board.

ECE 148 Analysis and Design of Digital Circuits *Spring 2017*

I am the instructor of for the department's course which teaches the analysis and design of digital circuits, both discrete and integrated circuits. Analysis and design is performed of solid state digital circuits utilizing various logic families suitable for integration such as TTL, ECL, NMOS, and CMOS. Digital circuits using these families are created, such as logic gates, multivibrators, ROM, PROM, EPROM, and EEPROM, SRAM and DRAM. This course builds on the analog circuits course by looking specifically at digital design and analysis.

Assistant Professor, California State University, Fullerton

EGCP 280 Microcontrollers *Fall 2016*

I am the instructor of for the program's microcontroller course. Microcontrollers are discussed, including microcontroller programming model and instruction set, assembler directives, writing and debugging microcontroller assembly language routines, microcontroller memory system, microcontroller communication systems. Microcontrollers are widely used in modern society with applications ranging in sophistication from simple toys to implantable medical devices. In this course, students will learn the principles of microcontrollers and learn how to use microcontrollers to implement digital systems. The primary microcontroller used in this course will be the Motorola 68HC12. The lab portion of this course aims to provide students with hands-on experience of programming and interfacing of the 68HC12 microcontroller.

EGCP 281 Designing with VHDL *Fall 2016*

I am the instructor for a section of the program's course teaching the basics of digital design with VHDL. The course is an introduction to various modeling methods, timings, events, propagation delays and concurrency, the language constructs, data representations and formats, and physical attributes. The course teaches VHDL, which is a Hardware Description Language, HDL, where digital designs are generally written then synthesized into standard cells, which are then fabricated into digital chips. In this course, students learn how to use one of these HDLs, namely VHSIC Hardware Description Language, or VHDL, to create basic digital designs, and to learn some design tradeoffs for different design methods.

EGCP 456 Introduction to Logic Design in Nanoelectronics *Fall 2016*

I am the instructor for the program's course on logic design in nanoelectronics. The course covers promising novel nanoelectronic technologies and logic primitives for such technologies, applicable basic logic design technique, design models for spatial dimensions, applicable word-level data structures, multilevel circuit design, testability and observability, tolerance and reliable computing. It is widely agreed upon that the scaling down of transistors for the current microelectronics technology cannot go below approximately 10 nm (transistor length) as fundamental and technological limits of conventional microfabrication and performance of microelectronic devices will be reached. This limit is expected to be reached by about 2020. Following the microelectronics era, new nanoelectronic devices must be expected to be at the forefront. Nanoelectronic devices will achieve higher levels of performance, functionality and capability that will hugely impact electronics, as well as signal processing and computing.

Lecturer, University of California, Davis

EEC 281 VLSI Digital Signal Processing *Winter 2016*

I am the instructor of record for the department's VLSI Digital Signal Processing course. I prepare and give lectures for the course as well as hold office hours and grade. This course covers digital signal processors, building blocks, and algorithms. It also covers design and implementation of processor algorithms, architectures, control, functional units, and circuit topologies for increased performance and reduced circuit size and power dissipation. The design projects in this course utilize Verilog HDL to design these DSP hardware implementations, and uses Cadence's Design Compiler to synthesize the HDL into gate level netlists for performance evaluation, using TSMC's 0.25 μm technology, with MOSIS design rules. The goal of the course is to impart the ability to design a processor for digital signal processing, with high-performance in mind, by exploring DSP algorithms, processor architecture, and hardware design.

Associate Instructor, University of California, Davis

EEC 116 VLSI Design *Fall 2015*

I was the instructor of record for the department's VLSI design course. I prepared and give lectures for the course as well as hold office hours. I supervised two teaching assistants who largely handle grading and holding office hours. This course covers CMOS devices, layout, circuits, and functional units; VLSI fabrication and design methodologies. It gives an introduction to the theory of CMOS gate operation and design. The course covers the theory and characteristics of CMOS transistors (NMOS and PMOS), including DC power, current, threshold voltage, body effect, channel width modulation, and timing. A broad overview of VLSI fabrication technologies is given, covering silicon wafer processing, transistor fabrication, interconnect, design rules, and future transistor process technologies.

Basic design methodology for creating custom VLSI circuits is also covered, using a tool flow including Magic, ext2sim, and IRSIM. Design tradeoffs are explored with simple CMOS circuits. VLSI design methodology of more complex circuits are covered, and culminates in a final project of a complex chip design, which uses information learned and functional modules created throughout the course.

Teaching Assistant, University of California, Davis

EEC 70 Computer Structure and Assembly Language *Winter 2013*

I managed multiple laboratory/office hour sections for the department's assembly language class, as well as writing lab assignments, leading review sessions, and proctoring exams. Lab assignments were centered on programing SPIM (an assembly simulator) in a progression of simplified assembly languages to teach the structure of computer systems. I graded weekly lab reports from my sections. I developed a new laboratory to be used in this and future classes as well as worked with the instructor to create the midterms and finals for the course.

EEC 116 VLSI Design *Fall 2012*

I managed multiple laboratory/office hour sections for the VLSI design class. Lab assignments were all completed using the Magic tool to draw transistors to make low level digital circuit designs. I graded lab reports and homework as well as giving help to students on VLSI theory and implementation.

EEC 70 Computer Structure and Assembly Language *Winter 2012*

See EEC 70 description above.

ENG 6 Engineering Problem Solving *Spring 2011*

I instructed two laboratory sections for the college's introductory programming course for all engineering majors. Classes started with a small lecture I prepared, and ended with a lab assignment/quiz. The class was based on Matlab, where the theory and basic programming ideas were taught by an instructor in a large class and specific instruction on Matlab was performed in the lab sections. I created labs, homework assignments, and exams as well as grading for my sections.

EEC 70 Computer Structure and Assembly Language *Winter 2011*

See EEC 70 description above.

Volunteer Tutor, University of California, Davis

Tau Beta Pi, CA-L Chapter *2009 – 2010*

I helped start a weekly free tutoring service as the advisor for UC Davis' Tau Beta Pi chapter, which is still ran by undergraduate student officers today. I volunteered my time tutoring students, mainly engineering lowerclassmen undergraduates in introductory programing classes and calculus.

Teaching Assistant, California State University, Fresno

ECE 1 Intro. to Electrical and Computer Engineering *Fall 2007 and Spring 2008*

I instructed multiple laboratory sections for the department's introduction class. Classes generally started with a small lecture/introduction I prepared, and proceeded to work time. Class projects were centered around programing microcontrolers on Boe-Bots to perform simple tasks. I graded weekly lab reports from my sections.

UNIVERSITY & PROFESSIONAL SERVICE

- Member of Technical Program Committee (TPC) for the "System Electronics, VLSI, and CAD" track of IEEE Conference on Dependable and Secure Computing (DSC 2017) *2017*
- Member of Program Curriculum Committee, Computer Engineering Program, CSU Fullerton *2016*
- Chapter Advisor of Tau Beta Pi, CA-L, UC Davis *2014 – 2009*
- Graduate Student Member of Transportation and Parking Administrative Advisory Committee, UC Davis *2014 – 2015*
- Chief Justice of Student Court, Associated Students Inc., CSU Fresno *2008*
- Chapter President of Tau Beta Pi, CA-R, CSU Fresno *2007*
- Senator on the Student Senate, Associated Students Inc., CSU Fresno *2006 – 2007*
- Student Member of Campus Planning Committee, CSU Fresno *2006 – 2007*
- Member of Board of Directors, University Union, CSU Fresno *2006 – 2007*
- Chapter President of Eta Kappa Nu, ΘK, CSU Fresno *2006*
- Reviewer
    - *IEEE Journal of Solid-State Circuits*
    - *IEEE Transactions on Very Large Scale Integration Systems*
    - *IFIP/IEEE International Conference on Very Large Scale Integration*
    - *IEEE Design and Test of Computers*
    - *IEEE/ACM International Symposium on Microarchitecture*
    - *IEEE International Conference on Computer Design*

PATENT

U.S. Patent Filed December 22, 2014

Application number 14/579,303
Assigned to Intel Corporation and U.S. Department of Energy
Gregory K. Chen, Mark A. Anders, Himanshu Kaul, Ram K. Krishnamurthy, and **Aaron T. Stillmaker**
"Combined Guaranteed Throughput and Best Effort Network-On-Chip"

AWARDS & HONORS

- GAANN Fellow *2008 – 2015*
- UC Davis ECE Dissertation Quarter Fellowship *Spring 2015*
- UC Davis ECE Graduate Program Fellow *2014*
- Graduate Studies Travel Award *2012*
- President's Scholar, Smittcamp Family Honors College *2004 – 2008*
- Graduate Student Member, IEEE
- Member, Tau Beta Pi
- Member, Eta Kappa Nu
- Member, Phi Kappa Phi

PUBLICATIONS & PRESENTATIONS

Aaron Stillmaker, Brent Bohnenstiehl, Lucas Stillmaker, and Bevan Baas, "Scalable Parallel Sorting on a Fine-Grained Many-Core Processor Array," In preparation.

This paper presents three sorting methods and two list exportation methods for the first phase of a 10 GB external sort with a fine-grained many-core processor array used as a co-processor with a laptop class processor, which computes the second phase. The proposed sorts are easily programmed and scalable to any sized 2D mesh processor array while giving a large energy savings without penalizing performance.

Aaron Stillmaker, and Bevan Baas, "Scaling Equations for the Accurate Prediction of CMOS Device Performance from 180 nm to 7 nm," *Integration, the VLSI Journal*. In press. Available online: February 13, 2017

This work presents CMOS device performance scaling factors between major technology nodes between 180 nm and 7 nm operating at voltages from 1.8 V to 0.5 V. The modeled performance scaling factors presented facilitates a fair, approximate comparison between VLSI designs fabricated in different technology nodes and using different supply voltages.

Brent Bohnenstiehl, **Aaron Stillmaker**, Jon Pimentel, Timothy Andreas, Bin Liu, Anh Tran, Emanuel Adeagbo, and Bevan Baas, "KiloCore: A Fine-Grained 1000 Processor Array for Task Parallel Applications," *IEEE Micro*. In press. **Invited.**

This invited paper will present the architectural details of KiloCore, a processor array containing 1000 independent processors and 12 memory modules was fabricated in 32nm PD-SOI CMOS.

Brent Bohnenstiehl, **Aaron Stillmaker**, Jon Pimentel, Timothy Andreas, Bin Liu, Anh Tran, Emanuel Adeagbo, and Bevan Baas, "KiloCore: A 32 nm 1000-Processor Computational Array," Submitted to *Journal of Solid-State Circuits*. In press. **Invited.**

This invited paper presents a processor array containing 1000 independent processors and 12 memory modules was fabricated in 32nm PD-SOI CMOS. The programmable

processors occupy 0.055 mm² each and operate up to an average maximum clock frequency of 1.78 GHz at 1.1 V. At 0.9 V, processors operating at a maximum average of 1.24 GHz dissipate 17 mW while issuing one instruction per cycle. Compared to a 22nm Intel i7, the 32nm KiloCore at 1.1 V averages 6.9x higher throughput and 27x higher energy efficiency for AES, 4095-bit LDPC, 4096-point complex FFT, and sorting applications.

Brent Bohnenstiehl, **Aaron Stillmaker**, Jon Pimentel, Timothy Andreas, Bin Liu, Anh Tran, Emanuel Adeagbo, and Bevan Baas, "KiloCore: A 32 nm 1000-Processor Array," In Proceedings of the *IEEE HotChips Symposium on High-Performance Chips, (HotChips 2016)*, Stanford, CA, August 2016.

This paper presents the design and architecture of the KiloCore 1000-Processor array. The chip, fabricated in 32 nm PD-SOI COMOS, contains 1000 programmable processors, as well as 12 independent memories.

Brent Bohnenstiehl, **Aaron Stillmaker**, Jon Pimentel, Timothy Andreas, Bin Liu, Anh Tran, Emanuel Adeagbo, and Bevan Baas, "A 5.8 pJ/Op 115 Billion Ops/sec, to 1.78 Trillion Ops/sec 32nm 1000-Processor Array," *IEEE Symposium on VLSI Circuits,* Honolulu, HI, June 2016.

This paper presents the first ever 1000-processor MIMD array. 1000 programmable processors and 12 independent 64KB memory modules capable of simultaneously servicing both data and instruction requests are integrated onto a 32nm PD-SOI CMOS device are presented. At 1.1V, processors operate up to an average of 1.78GHz which implies a maximum chip throughput of 1.78 trillion ops/sec. At 0.84V, 1000 cores process 1 trillion ops/sec at 13.1 W.

Aaron Stillmaker, "Design of Energy-Efficient Many-Core MIMD GALS Processor Arrays in the 1000-Processor Era," Ph.D. Dissertation, University of California, Davis, December 2015.

This dissertation offers three different novel methods to perform a high throughput energy-efficient database sort data records using a fine-grained many-core processor array. The dissertation presents the developed physical design flow and design methodology for creating a digital chip in the 1000-processor era. A number of design considerations are discussed, including module design, power grid design, power gate system design, physical DVFS requirements, communication, and chip level layout. The design for both KiloCore and KiloCore2 are covered, as well as preliminary measured results from KiloCore, the first fabricated chip containing 1000 MIMD, programmable, independent processing cores on a single die. Early results show that KiloCore can perform at 5.8 pJ/Op at 115 Billion Ops/sec at 0.56 V, and up to 1.78 Trillion Ops/sec at 1.1 V. KiloCore2 contains 697 programmable processors, two of which are optimized for high speed, one fast Fourier transform accelerator, and two Viterbi decoder accelerators.

Jon Pimentel, **Aaron Stillmaker**, Brent Bohnenstiehl, and Bevan Baas, "Area Efficient Backprojection Computation with Reduced Floating-Point Word Width for SAR Image Formation," *Asilomar Conference on Signals, Systems, and Computers*, 2015, Asilomar, CA, November, 2015.

This paper proposes reducing the floating-point word size for an algorithm for airborne synthetic aperture radar backprojection image formation. The circuit area in 65 nm CMOS and the PSNR and SSIM metrics are found for 572 design points. With word-width reductions of 44.4–81.3%, images with a 0.99 SSIM are created with imperceptible image quality degradation and a 2.7–15.9x reduction in area.

Aaron Stillmaker, Brent Bohnenstiehl, Jon Pimentel, and Bevan Baas, "Energy-Efficient and High Performance Many-Core Arrays," *SRC System Level Design Review*. Hillsboro, OR, May 2015.

This poster presentation was given at the annual SRC review for the System Level Design thrust. The information given was on recent and ongoing research in many-core arrays, including work on many-core architecture, design and applications.

Zheng Cao, Roberto Proietti, **Aaron Stillmaker**, Nima Mostafavi, Bevan Baas, and S. J. Ben Yoo, "Energy-Efficient, High-Performance, and Reliable Computing with Massively Parallel AsAP and Interconnects," *ACS Productivity Workshop*, Catonsville, MD, July 2014.

Presentation describing the joint work from Prof. Baas and Prof. Yoo's groups on using high bandwidth optical interconnects to network a large array of many-core processors together to perform enterprise applications inside of large server data centers.

Aaron Stillmaker, "Energy-Efficient Sorting on a Many-Core Processor Array." Invited Talk, Intel (Intel Labs: Circuit Research Lab), Hillsboro, OR, September 2013.

This presentation was on my current and ongoing research in the area of energy-efficient sorting on a many-core processor array given to the Circuit Research Lab at Intel Labs at the beginning of my internship.

Aaron Stillmaker, Lucas Stillmaker, Brent Bohnenstiehl, and Bevan Baas, "Energy-Efficient Sorting on a Many-Core Platform," *Technology and Talent for the 21st Century (TECHCON 2013),* Austin, TX, September 2013.

As processors move from multi-core to many-core architectures, opportunities arise for energy-efficient enterprise computations, such as sorting, on large arrays of processors. This paper proposes three different energy-efficient sorting methods for the first phase of an external sort simulated on a varying sized fine-grained many-core processor arrays used as a co-processor to an Intel CPU, which completes the second phase. Preliminary results are shared in this short paper, poster, and presentation.

Aaron Stillmaker, "Energy-Efficient Sorting on a Many-Core Processor Array." Invited Talk, Oracle (Sun Microsystems), Santa Clara, CA, March 2013.

This presentation was on my current and ongoing research in the area of energy-efficient sorting on a many-core processor array given to the Software-in-Silicon research and development group in what used to be Sun Microsystems, and is now a division of Oracle.

Aaron Stillmaker, Lucas Stillmaker, and Bevan Baas, "Fine-Grained Energy-Efficient Sorting on a Many-Core Processor Array," *IEEE International Conference on Parallel and Distributed Systems (ICPADS 2012),* Singapore, December 2012.

Data centers require significant and growing amounts of power to operate, and with increasing numbers of data centers worldwide, power consumption for enterprise workloads is a significant concern. We propose two highly parallel sorting algorithms and mappings using a modular design for a fine-grained many-core system that greatly decreases the amount of energy consumed to perform sorts of arbitrarily large data sets. We present the design and implementation of several sorting variants that perform the first phase of an external sort. They are built using program kernels operating on independent processors in a many-core array with 256 bytes of data memory and fewer than 128 instructions per processor.

Aaron Stillmaker, and Bevan Baas, "Modular Sorting on a Fine-Grained Many-Core Processor Array," *Industrial Affiliates Conference,* Davis, CA, June 2012.

This presentation was on my current and ongoing research in the area of energy-efficient sorting on a many-core processor array presented as a poster for ECE Department's Industrial Affiliates Conference.

Aaron Stillmaker, Zhibin Xiao, and Bevan Baas, "Toward More Accurate Scaling Estimates of CMOS Circuits from 180 nm to 22 nm," Technical Report ECE-VCL-2011-4, VLSI Computation Laboratory, ECE Department, University of California, Davis, December 2011.

With deep submicron technology nodes other methods are needed to obtain scaling factors rather than the traditional scaling factors, which held for the pre-submicron era. This work presents scaling factors between major technology nodes between 180 nm and 22 nm operating at voltages from 1.8 V to 0.7 V. Common operating data for these technologies were taken from the International Technology Roadmap for Semiconductors (IRTS). HSpice simulations that rely on the Predictive Technology Model (PTM) for transistor characteristics were used to find the scaling factors.

Aaron Stillmaker, Zhibin Xiao, Bin Liu, and Bevan Baas, "Computing Enterprise Workloads With Many-Core Arrays as Special-Purpose Processors," *C2S2 Annual Review,* Atlanta, GA, October 2011.

This presentation was on our research group's current and ongoing research in the area of using many-core processor arrays for enterprise workloads. My efforts with regular expression operations as well as ongoing research on many-core sorting algorithms were showcased in the presentation.

Aaron Stillmaker, Zhibin Xiao, and Bevan Baas, "Computing Enterprise Workloads With Many-Core Arrays and Special-Purpose Processors," *C2S2 Annual Review,* Atlanta, GA, October 2010.

This presentation was on our research group's current and ongoing research in the area of using many-core processor arrays for enterprise workloads. My beginning research on many-core sorting algorithms was showcased in the presentation.

TOOLS/SKILLS

- HDL Tools: Cadence NC Verilog, Cadence Verilog XL, ModelSim
- HDL Languages: Verilog, VHDL
- RTL Gate-Level Synthesis: Synopsys Design Compiler
- Place and Route: Cadence SoC Encounter
- Custom Layout: Cadence Virtuoso, Magic VLSI Layout Tool
- Circuit Simulation: Synopsys HSpice, Synopsys PrimeTime, IRSIM
- DRC and LVS Tool: Mentor Graphics Calibre
- Assembly Languages: MIPS, x86, HC12
- Programing Languages: C, C++, CUDA, Java, Perl, Bash, TCL
- Numerical Computing Environment: Matlab
- Miscellaneous: Unix, LaTeX

RELEVANT COURSEWORK

Graduate

- Low Powered Digital IC
- DSP VLSI Design
- Design and Optimization of Embedded Systems
- Graphics Architecture
- Digital Signal Processing
- Digital Image Processing
- Code Generation
- High Performance Computer Architecture
- Advanced Computer Architecture

Undergraduate

- Advanced Computer Architecture
- Digital Logic and System Design
- VLSI Design
- Programming in C and C+
- Analog Circuit Analysis
- Signals and Systems
- Computer System Architecture Organization
- Digital Signals Processing
- Random Signals Analysis
- Verilog HDL
- Computer Processor Architecture
- Computer Networks and Distributed Processing
- Operating Systems
- Software Engineering